A TEST BOARD FOR MULTIPORT IMMITTANCE MEASUREMENT AND CHARACTERIZATION OF RF-IC PACKAGES

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Abstract— **An experimental technique based on the measurement of two port scattering parameters for the characterization of electrically small RF-IC package is presented. The procedure is based on a novel test board design to facilitate extraction of n-port admittance and impedance matrix parameters using two port network analyzer scattering parameter measurements. An optimization routine is used to extract the SPICE based equivalent circuit model that includes the mutual coupling effects present in the RF-IC package pins.**

I. Introduction

Accurate electrical characterization of RF-IC plastic packages is an important issue in the design of Silicon and GaAs based wireless communication systems. With the increase in frequency and integration of more functionality, the parasitics associated with these RF-IC packages now play a dominant role in the performance of integrated circuits (on die) and therefore need to be included during the design cycle. Several experimental techniques based on time and frequency domain measurements [1,2,3] and rigorous EM tools [4,5] have been proposed to characterize the parasitics associated with the RF-IC packages in terms of lumped and distributed equivalent SPICE based models. The CPW based wafer probe technique [1] is excellent for the extraction of accurate self parasitic values but not for the mutual inductances and capacitances between adjacent pins. Also, unlike a previously used time domain technique [2] based on TDR, which provides wide band characterization of RF-IC parasitics with the limited dynamic range of TDR, the frequency domain characterization procedure presented in this paper is applicable to narrow band characterization, needed for RF-IC applications. Further, the frequency dependent skin effect losses of the RF-IC pins and the associated dielectric losses can also be included in the extracted equivalent circuit SPICE model.

In this paper a measurement based technique in frequency domain is presented to extract equivalent circuit SPICE model of electrically small low cost RF-IC plastic packages used in wireless communication systems. The extracted SPICE model includes all the mutual coupling effects present in the RF-IC package pins.

II. Extraction Procedure

An electrically small (dimensions are very small compared to the operating wavelength) RF-IC package with n pins corresponds to a $2n$ port system. In general one end of each pin (paddle side end) does not have access to a suitable ground reference, restricting the usage of on die calibration structures [1]. Moreover, for the accurate characterization of RF-IC packages, the measurement setup requires an environment similar to that of an IC placed on the actual manufacturing board. The above requirement arises due to the significant dependence of equivalent circuit SPICE model values (L,C's etc.) on the board parameters. Additionally, the board parameters such as ϵ_r, dielectric losses,

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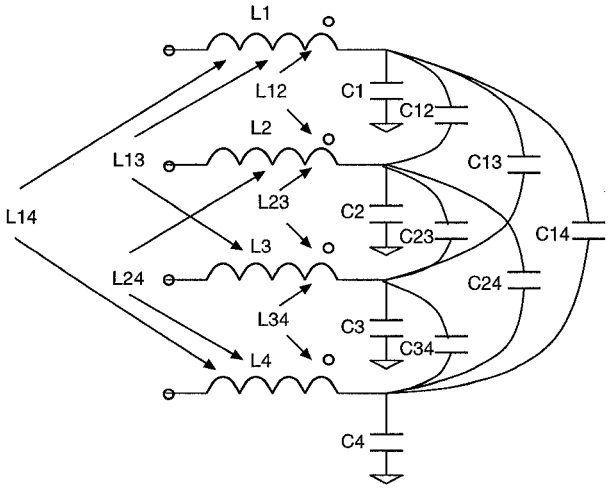
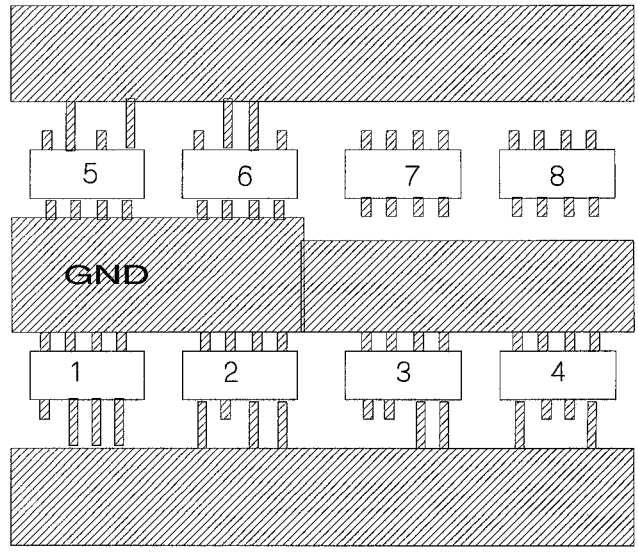


Fig. 1. Equivalent circuit model for the package pins (8 pins SOIC package).



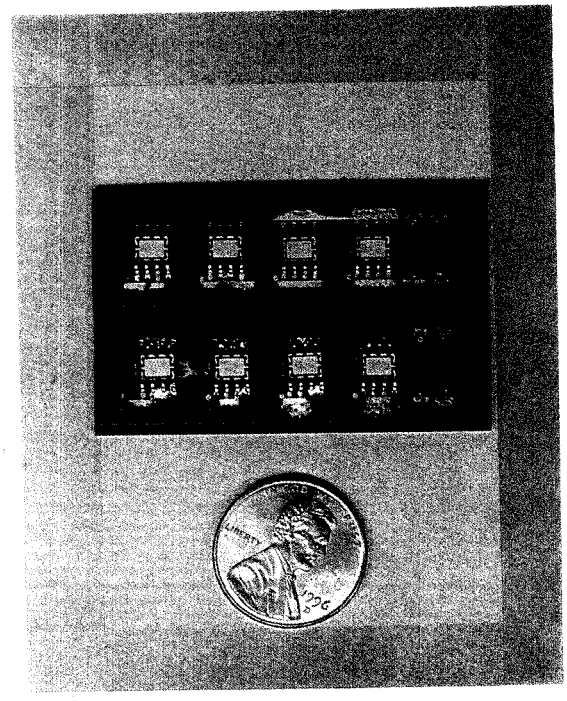
(a)

via inductance etc., are the required specifications to be determined for the package model. Furthermore, the electrically small size of an RF-IC package leads to an equivalent SPICE model in terms of lumped circuit elements (R,L,C) which in turn is adequate for the design and simulation of the package with CAD tools. It is to be noted that for electrically small structures such as RF-IC packages, capacitive coupling among the pins dominates when high impedances are connected to the IC pin ends. Similarly, inductive coupling dominates when low impedances are connected to the pin ends.

A. Measurement Board: Design

For the extraction of the equivalent circuit shown in Fig. 1, the following observations are utilized in the design of the measurement board :

- Self capacitance dominates in the measurement when all other pins of the RF-IC package are shorted to the ground. The measured self capacitances are given by, $C_{ii} = C_{meas} - \sum_{j=1, j\neq i}^{n} C_{ij}$, where n is the number of IC pins. The pins on which the self capacitance measurements are done are left open-circuited.



(b)

Fig. 2. a) Measurement board layout. b) The actual measurement board according to the layout in fig. 2a.

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- The mutual capacitances dominate in the measurement when all other pins of RF-IC package are shorted to the ground. The mutual capacitances are given by $C_{ij} = C_{meas}$ from two port measurement. The pins i and j across which mutual capacitance measurement is performed are left open.

- In the case of self and mutual inductance measurements all the other pins of the RF-IC package are left open. The pins across which the mutual or self inductance measurement is performed are connected to the paddle with bond wires of known lengths. The paddle is suitably connected to the ground by removing the plastic beneath the paddle and then providing a suitable low inductance ground contact. The inductance of this ground contact is later deembedded from the measurement.

A typical measurement board for an eight pin RF-IC package is shown in Fig. 2a and the actual board designed according to the layout (Fig. 2a) is shown in Fig. 2b. IC packages placed in positions 1 and 2 provide the estimate of the first order approximate values of self capacitances. IC packages placed in positions 3, 4, 5 and 6 are used to estimate first order approximate values of mutual capacitances. Likewise, IC packages placed over positions 7 and 8 provide the estimate of first order approximate values of self and mutual inductances. It is to be noted that the IC package placed on positions 7 and 8 (Fig. 2a) are connected to the paddle with the bond wires of known lengths.

III. Results

A simple equivalent circuit model for the paddle connected to the ground, bond wires and two package pins is shown in Fig. 3. The values of the inductances Lx_{ij} in the paddle model (paddle inductance from ith pin to jth pin) are small and therefore neglected. Furthermore, the inductance arising from the ground connection of the paddle is assumed to be the same for each pin. The impedance matrix ($[Z(\omega)]_{4\times4}$) and the admittance matrix ($[Y(\omega)]_{4\times4}$) are obtained by measuring the two port S parameters of IC packages placed over positions 1 to 8 on the measurement board. Using

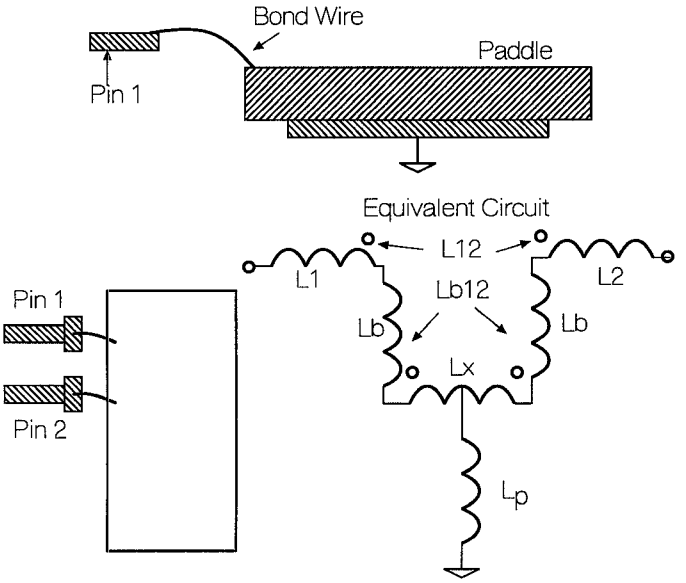

Fig. 3. Electrical equivalent circuit for the paddle in the measurement setup (Lx is very small and Lp is constant for each pin).

Table: 1

Measured Capacitances (pF), frequency: 2Ghz

	Pin 1	**Pin 2**	**Pin 3**	**Pin 4**
Pin 1	**0.300**	**0.031**	**0.0027**	**0.0006**
Pin 2	**0.031**	**0.27**	**0.029**	**0.0027**

Measured Inductances (nH), frequency: 2Ghz

	Pin 1	**Pin 2**	**Pin 3**	**Pin 4**
Pin 1	**1.95**	**0.53**	**0.196**	**0.042**
Pin 2	**0.53**	**1.58**	**0.44**	**0.196**

Lp (paddle to ground inductance)=0.2nH (2GHz)

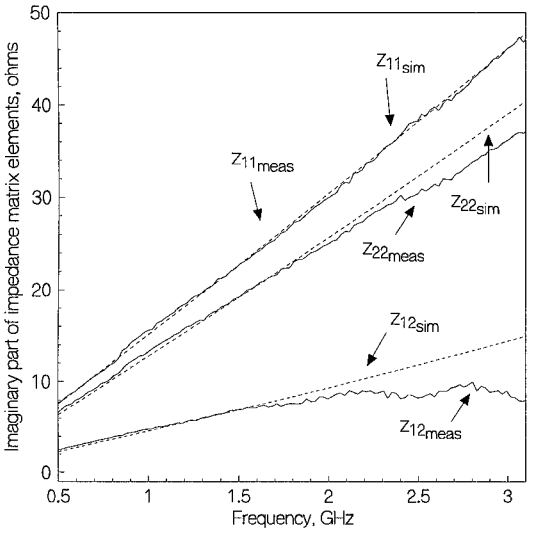

Fig. 4. Plot of the measured and the simulated (with SPICE model) impedance matrix elements Z_{11} Z_{12} and Z_{22} of the SOIC package pins 1 and 2 as a function of frequency.

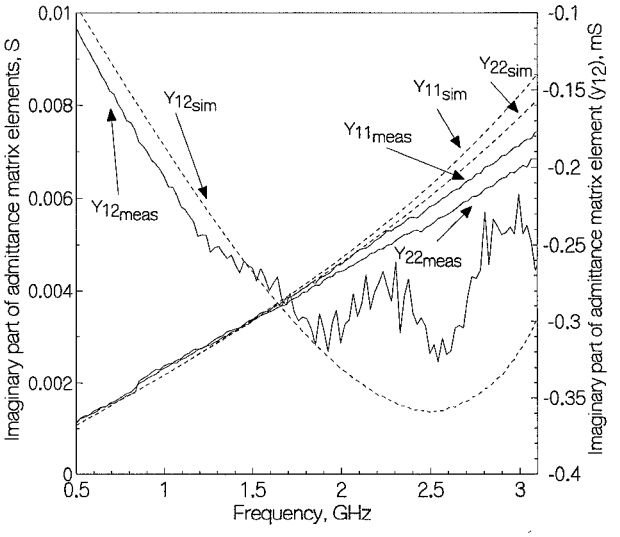

Fig. 5. Plot of the measured and the simulated (with SPICE model) impedance matrix elements Y_{11} Y_{12} and Y_{22} of the SOIC package pins 1 and 2 as a function of frequency.

the estimated values of mutual and self capacitances and inductances as an initial guess in an optimization routine, all the values of lumped elements present in the equivalent SPICE model circuit (Fig. 1) are extracted. The typical values obtained for an 8 pin SOIC RF-IC package with the grounded paddle are shown in Table 1. Figures 4 and 5 show the comparison between the measured and the simulated (with SPICE model) impedance and the admittance matrix elements Z_{11}, Z_{12}, Z_{22}, Y_{11}, Y_{12} and Y_{22} of the SOIC package pins 1 and 2.

IV. Conclusion

An extraction procedure suitable for accurate electrical characterization of electrically small RF-IC packages is presented. The procedure utilizes a suitable board fixture and Cascade Microtech coplanar waveguide probes (CPW) for measurement of two port S parameters leading to the extraction of an n port impedance and admittance matrix. An optimization routine is then used to obtain the equivalent SPICE model. It is observed that the simulated results obtained from the SPICE model are in good agreement with the measured data.

Acknowledgment

This work was supported in part by HP EEsof, Santa Rosa, Ca.

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